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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/661,223	09/13/2000	Futoshi Kaibuki	450100-02710	7775

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EXAMINER
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HUYNH, KIM T

ART UNIT	PAPER NUMBER
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2112

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

## Application No.

09/661,223

## Applicant(s)

KAIBUKI, FUTOSHI

## Examiner

Kim T. Huynh

## Art Unit

2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 13 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,3,6,9-13,15-19,21,24-26,28 and 30-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,6,9-13,15-19,21,24-26,28 and 30-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 September 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Receipt Acknowledgement*

1. Receipt is acknowledged of the request filed on 13<sup>th</sup> of January 2005 for a request for continued examination (RCE) under 37 CFR 1.114 based on the application No. 09/661223, which the request is acceptable and an RCE has been established. Claims 2, 4-8, 14-16, 20, 22-25, 27, 29-31, 33 have been canceled. Currently, claims 1, 3, 9-13, 17-19, 21, 26, 28, 32 are pending in this application.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3, 6, 9-13, 15-19, 21, 24-26, 28, 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ludtke et al. (Pub. No US 20030210252) in view of Washino (US Patent 6,370,198)

As per claims 1, 19, Ludtke discloses an electronic apparatus for processing audio/video data, comprising:

- A data processing subunit(fig.3, 60 ie TV), included within said electronic apparatus, for receiving and processing audio/video input data; [0039], [0015]

- A first functional block (fig.3, 64, ie VRAM), included within said data processing subunit, operative as an audio/visual processing functional block to process the audio/visual input data; [0039-0043]
- A second functional block (fig.3, 62, ie display), included within said data processing subunit, operative as terminating functional block to terminate the data processed by said first functional block by transforming the audio/visual data into a user-visible signal and outputting said user-visible signal being not processed afterward; [0039-0043], ie, the subunit 60 loads packet within the buffer 78 into the VRM circuit 64 (first functional block) to be shown on the display 62 (second functional block)
- A memory (fig.3, 78 ie buffer) for storing information pertaining to said data processing subunit and said second functional block, wherein the information stored in said memory is accessible by an external electronic apparatus connected to said electronic apparatus via a serial data bus; and [0014],[0018],[0039]
- Connection means for connecting said electronic apparatus and said external electronic apparatus via said serial data bus. [0014]
- Wherein said information pertaining to said first and second functional blocks stored within said memory includes type information of said first and second functional blocks and virtual plug information of said first and second functional blocks and the virtual plug information of said second functional block contains information indicating that the input plug of said

second functional block is connected to said first functional block. (figure 3, [0039-0043] discloses data loaded into memory locations within the buffer 78 corresponding to the address value contained within the packet. The subunit 60 loads packet within the buffer 78 into the VRM circuit 64 to be shown on the display 62. This implies virtual plugging of connection second functional block to first functional block.)

Ludtke discloses all the limitations as above except by transforming the data to an image signal. However, Washino discloses interface unit operative to convert the video program in the input format into an output signal representative of formatted image, and output the signal to an attached display device. (col.4, lines 27-40)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Washino's teaching into Ludtke's system so as to provide capabilities of high performance personal computer or workstation. (col.4, lines 1-6)

As per claims 3, 21, 28, Ludtke discloses wherein the information stored in said memory indicates that said functional block terminates data received by the data processing subunit.[0018]

As per claim 9, Ludtke discloses wherein said memory has a hierarchical structure.(fig.3, [0039-0043]

As per claim 10, Ludtke discloses wherein said data is video data and said second functional block is a video display means that terminates said video data

by converting the processed data into a video signal and displaying video corresponding thereto. [0007-0009]

As per claim 11, Ludtke discloses wherein said video display means is a display. [0040]

As per claim 12, Ludtke discloses wherein said video display means is a printer.

As per claim 13, Ludtke discloses wherein said data is audio data and said second functional block is an audio output means that terminates said audio data by converting it into sound corresponding thereto. [0007]

As per claim 17, Ludtke discloses wherein said serial data bus performs data communication in accordance with the IEEE-1394 standard. [0040]

As per claim 18, Ludtke discloses wherein said electronic apparatus is a digital television receiver. [0040]

As per claims 26, 32, Ludtke discloses a system having a plurality of electronic apparatuses connected via a serial data bus to enable transmission of data among said apparatuses, comprising:

- A data transmitting apparatus for transmitting audio/video data over said serial data bus; [0039], [0018]
- A data receiving apparatus for receiving the audio/video data transmitted by said serial data transmitting apparatus over said data bus; [0018]

Wherein said data receiving apparatus comprises:

- A data processing subunit, included within said receiving apparatus, for processing said received audio/video data; [0039]

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- A first functional block (fig.3, 64, ie VRAM), included within said data processing subunit, operative as an audio/visual processing functional block to process the audio/visual input data; [0039-0043]
- A second functional block (fig.3, 62, ie display), included within said data processing subunit, operative as terminating functional block to terminate the data processed by said first functional block by transforming the audio/visual data into a user-visible signal and outputting said user-visible signal being not processed afterward; [0039-0043], ie, the subunit 60 loads packet within the buffer 78 into the VRM circuit 64 (first functional block) to be shown on the display 62 (second functional block)
- A memory for storing information pertaining to said data processing subunit and said second functional block, wherein the information stored in said memory is accessible by an external electronic apparatus connected to said electronic apparatus via said serial data bus. [0039], [0014], [0018]
- Wherein said information pertaining to said first and second functional blocks stored within said memory includes type information of said first and second functional blocks and virtual plug information of said first and second functional blocks and the virtual plug information of said second functional block contains information indicating that the input plug of said second functional block is connected to said first functional block. (figure 3, [0039-0043] discloses data loaded into memory locations within the

buffer 78 corresponding to the address value contained within the packet. The subunit 60 loads packet within the buffer 78 into the VRM circuit 64 to be shown on the display 62. This implies virtual plugging of connection second functional block to first functional block.)

Ludtke discloses all the limitations as above except transforming the data to an image signal. However, Washino discloses interface unit operative to convert the video program in the input format into an output signal representative of formatted image, and output the signal to an attached display device. (col.4, lines 27-40)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Washino's teaching into Ludtke's system so as to provide capabilities of high performance personal computer or workstation. (col.4, lines 1-6)

#### ***Response to Amendment***

4. Applicant's amendment filed on 1/13/05 have been fully considered but does not place the application in condition for allowance.

a. Applicant argues that nothing has been found in the cited portions of Ludtke or Washino, taken alone or in combination, that would teach or suggest a second functional block that terminates the data processed by said first functional block. Examiner respectfully disagrees. As Ludtke notes in figure 3, [0039-0040], discloses the television 60 (subunit) included VRAM circuit 64(first functional block) receiving and processing data for the display (second functional block). Thus, the prior art teaches the



invention as claimed and the amended claims do not distinguish over the prior art as applied.

b. Furthermore, Applicant argues that nothing in Ludtke or Washino teaches or suggests virtual plug information of second functional block contains information indicating that the input plug of said second functional block is connected to said first functional block. Examiner again respectfully disagrees. As Ludtke notes in figure 3, [0039-0043] discloses data loaded into memory locations within the buffer 78 corresponding to the address value contained within the packet. The subunit 60 loads packet within the buffer 78 into the VRM circuit 64 to be shown on the display 62. This implies connection second functional block to first functional block. Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

### **Conclusion**

5. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9:00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at (571)272-3632 or via e-mail addressed to [mark.Rinehart@uspto.gov].*

*The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.*

Kim Huynh

March 31, 2005



**TIM VO**  
**PRIMARY EXAMINER**